MSG 39 815 ECJ FEJP CJP ALCC
TO: RYOJI YONEMOTO.....FEJP

CC: YUICHI MURANO.....ECJ
CHUCK BRANSON.....ALCC
DARRELL WHITTEN.....HEXB

FM: C.B. WILSON.....ALC1

RE: 70C20A

WE ARE STILL CONTINUING TO TRY TO FIND OUT WHAT THE REAL PROBLEM IS WITH THE SOFTWARE WE HAVE IN THE 70C20 FOR THE WAFERTAPE (GATE CODE L11001). AS I MENTIONED TO YOU WHEN I WAS IN JAPAN, WE GET A FAILURE USING THE ACTUAL PART THAT WE DON'T SEEM TO GET WHEN USING THE AMPL. SINCE THAT TIME WE HAVE FOUND A SERIOUS PROBLEM WITH OUR MACHINE LEVEL CODE, BUT THAT ERROR DOES NOT EXPLAIN WHY THE AMPL WORKS AND WE BELIEVE A SEPARATE PROBLEM IS RESPONSIBLE FOR THE ACTUAL FAILURE.

IN SEARCHING FOR THIS SECOND FAILURE, WE HAVE BEEN TESTING SOME CODE (WHICH DOES NOT USE THE MICROCODED INSTRUCTIONS OF THE L11001) ON THE 70C20A. WE ARE APPARENTLY SEEING A SUPRIZING FAILURE ON THESE 70C20A PARTS. THE FAILURE APPEARS TO BE THAT THE PART IS NOT ABLE TO BE INTERRUPTED OUT OF AN IDLE STATE WITH AN INTERRUPT 2 FROM THE TIMER. SPECIFICALLY, WE HAVE THE FOLLOWING CODE:

```
        MOVP   %START,TIMER     START = >A0, TIMER  = >03
        MOVP   %I2CS,IOCNTL     I2CS  = >4C, IOCNTL = >00
        EINT
        CLR B
        IDLE
        BTJO %SETBIT,B,RSYNC8
```

THE FAILURE WE BELIEVE WE ARE SEEING IS THAT THE PART DOES NOT EVER COME OUT OF THE IDLE INSTRUCTION WHEN THIS IS EXECUTED. I AM NOT ABSOLUTELY SURE OF THIS BECAUSE WE HAVE ONLY A COUPLE OF 70C20A PARTS OVER HERE AND THIS WAS NOTICED LATE FRIDAY FOR THE FIRST TIME. WE HAVE SOME OTHER 70C20A PARTS OVER IN THE QUAL LAB WHICH I WILL GET BACK MONDAY AND WE WILL VERIFY AGAIN WITH MORE PARTS AND MAKE ABSOLUTELY SURE WE ARE NOT SEEING SOMETHING ELSE. IT IS DIFFICULT FOR ME TO IMAGINE THAT THE PART ACTUALLY HAS THIS TYPE OF FAILURE, BUT I WANTED TO ADVISE YOU OF OUR INFORMATION AND GET YOUR COMMENT.

I AM STILL INTERESTED VERY MUCH IN THE PROGRESS OF THE LOTS OF WAFERTAPE CODE ON THE 70C20A (GATE CODE L71000S). DO YOU HAVE ANY CHANGE TO THE 11/2 SHIPPING DATE FOR THESE PARTS?

BEST REGARDS,
C.B. WILSON.....ALCC/ALC1

-MSG M#= 114706 FR=ALCC TO=ALCC SENT=10/14/83 06:55 PM
R#=043 ST=C DIV=039 CC=0815 BY=JHPE AT=10/06/83 09:09 PM
TO: C B WILSON - ECJ
TO: JIM ARNORD - ALCC
CC: I KOIKE - AKRI
CC: Y UCHIDA / S SATO - FEJP

RE: L11001 REPLY FOR YOUR TELEPHONE CALL

((DEVICE STATUS))
GATE CODE NEME OF C20A (PREVIOUSLLY CALLING L11001) IS L71000S.
2 LOTS OF L71000S PARTS ARE RUNNING AT OUR FRONT-END,AND SHIPPING
COMMITMENT ARE AS FOLLOWS.

SLICE OUT	10/26
F.G OUT	11/1
SHIPPING	11/2

PROBABLY SAME AS C71003 SHIPPING WHICH PARTS WERE PREVIOUSLLY CALLING
THE GATE CODE C11006.

((FUNCTION DIFFERENCE BETWEEN C20A AND C20))

	C20	C20A
- PRIORITY OF INT CLR AND EN	X	O
- ILLEGAL RELEASE OF IDLE STATE	X	O

X ----- NOT CORRECT
O ----- CORRECT

= DETAILS OF PRIORITY OF INT CLR AND EN =
I/O CONTROL REGISTOR SET "1 1" (CLR/EN AT THE SAME TIME),IN THIS CASE,
IF INT INPUT IS ALREADY LATCHED AND INT FLG IS ACTIVE,IT IS ORDINARY
MANNER TO CLEAR INT FLG PRIOR TO ACCEPT INTERRUPT WITH EN FLG="1"
AND DISABLE INTERRUPT ACTION.
HOWEVER C20 WILL OCCASIONALLY PRIORITIZE EN BIT AND ACTIVE INTERRUPT
DUE TO TIMING SKEW.
= DETAILS OF ILLEGAL RELEASE OF IDLE STATE =
WHEN CPU EXECUTES IDLE INSTRUCTION,CPU ENTERS INTO POWER SAVE MODE BY
CLOCKHALT.THE RELEASE OF THIS STATE WILL BE DONE BY INT INPUT.
IF THE INT INPUT NOT INFLUENCED BY INT BIT AT STATUS REGISTOR OR INT EN
BIT IS USED,IT WILL CREATE THE PROBLEM.
FOR EXAMPLE,AT THE STATE THAT INT3 IS DISABLE BY EN BIT OF I/O CONTROL
REGISTOR,INT3 INPUT BECOMES ACTIVE FOR IDLE RELEASE,CPU NEVER ENTERS
TO INT3 ROUTINE WHILE CLOCK KEEPS RUNNING.WHEN INT IS DISABLED BY INT
BIT OF STATUS REGISTOR,THE SAME THING MAY HAPPEN.

BEST REGARDS.
RYOJI YONEMOTO FEJP

```
      F504  02
1067  F505  92          MOVP   B,TIME                  2/3 bit timer
      F506  02
1068  F507  D5          CLR    CHKSUM                  set chksum to 0
      F508  31
1069  F509  D5          CLR    CHKSUM-1
      F50A  30
1070              *       COPY   ALC.JCF.STRINGY.SRC.OLDRINT   old microcode i
1071  F50B  72          MOV    %RBITDT/256,INT2V-1
      F50C  F7
      F50D  33
1072  F50E  72          MOV    %RBITDT-(256*(RBITDT/256)),INT2V
      F50F  8A
      F510  34
1073              *       MOV    %RDBIT1,INT2            set up INT2 opcode
1074              *       MOV    %RDBIT2,INT2+1          set up INT2 parameter
1075              *       CLR    INT2+2                  set up INT2 parameter
1076  F511  A2          MOVP   %START,TIMER            start 2/3 bit timer
      F512  A0
      F513  03
1077  F514  A2          MOVP   %I2CS,IOCNTL            select & clear INT2
      F515  4C
      F516  00
1078  F517  05          EINT                           reinterruptidity
1079  F518  C5          CLR    B                       TEST
1080  F519  01          IDLE                           TEST
1081  F51A  56          BTJO   %SETBIT,B,RSYNC8        test for 1
      F51B  08
      F51C  05
1082  F51D  C5  RSYNC7  CLR    B                       TEST
1083  F51E  01          IDLE                           TEST
1084  F51F  57          BTJZ   %SETBIT,B,RSYNC9        test for 0
      F520  08
      F521  07
1085  F522  C5  RSYNC8  CLR    B                       TEST
1086  F523  01          IDLE                           TEST
1087  F524  57          BTJZ   %SETBIT,B,RSYNC7        test for 0
      F525  08
      F526  F6
1088  F527  E0  RESINK  JMP    RESYNC                  if two 1's in a row
      F528  89
1089              * test for 2 more 0s
1090  F529  C5  RSYNC9  CLR    B                       TEST
1091  F52A  01          IDLE                           TEST
1092  F52B  56          BTJO   %SETBIT,B,RESINK        test for 1
      F52C  08
      F52D  F9
1093  F52E  C5          CLR    B                       TEST
1094  F52F  01          IDLE                           TEST
1095  F530  56          BTJO   %SETBIT,B,RESINK        test for 1
      F531  08
      F532  F4
1096  F533  72          MOV    %4,BITCON               bitcon will have been 1
      F534  04
      F535  02
1097  F536  EE          TRAP   BIT8BA                  wait end of nibble (spac
1098              * register A will have been swapped (spacer only)
```

```
 0204                *-------------------------------------------------------
 0205                * wafer drive control constant equates
 0206      00FF      INITDR EQU    >FF                    initialize drive
 0207      0001      INITWF EQU    >01                    initialize wafer ddr
 0208      00F3      MT     EQU    >F3                    turn on motor & sensor
 0209      0008      MTBAR  EQU    >08                    turn off motor
 0210      00F1      MTWE   EQU    >F1                    turn on motor, WE & sens
 0211      0000      RENITW EQU    >00                    tri-state DO
 0212      00FB      SN     EQU    >FB                    turn on EOT/BOT sensor
 0213      00FB      STOP   EQU    >FB                    turn off drive except se
 0214      00F9      WE     EQU    >F9                    turn on WE & sensor
 0215                * wafer test contant equates
 0216      0040      BATTRY EQU    >40                    bit-test for battery-lev
 0217      0002      EOTTST EQU    >02                    bit-test for EOT
 0218      0080      INPUT  EQU    >80                    bit-test for input data
 0219      0004      WP     EQU    >04                    bit-test for WP
 0220                * wafer data consatnt equates
 0221      0001      INVBIT EQU    >01                    wafer-write invert
 0222      0008      SETBIT EQU    >08                    store a "1" bit
 0223                *-------------------------------------------------------
 0224                * bus control constant equates
 0225      0001      DROP   EQU    >01                    drop HSK bit
 0226      0000      HSKSET EQU    >00                    let HSK float
 0227      0004      INHIB  EQU    >04                    inhibit IBC
 0228      0001      RELEAS EQU    >01                    release-HSK bit
 0229                * bus test constant equates
 0230      0001      HSK    EQU    >01                    bus ready bit-test
 0231      0008      IRQ    EQU    >08                    bus data ready bit-test
 0232      0002      BAV    EQU    >02                    BAV active test
 0233                *-------------------------------------------------------
 0234                       COPY   ALC.JCF.STRINGY.SRC.MHZ358
B0001                * timer constant equates
B0002      000D      BITIME EQU    >0D    3.58MHz,8KBaud  data half-bit time
B0003      0020      HALT   EQU    >20                    stop timer
B0004      00C0      HRANGE EQU    >C0    3.58MHz         high time/low freq cutof
B0005      0038      LRANGE EQU    >38    3.58MHz         low time/high freq cutof
B0006      00BF      MAX    EQU    >BF                    max timer, no sleep
B0007      0006      ORANGE EQU    >06    3.58MHz         bit to bit compare
B0008      0000      SLEEP  EQU    >00                    sleep mode
B0009      00A0      START  EQU    >A0                    timer-start bit
B0010                * software loop constants
B0011      0067      BOSTIM EQU    >67    3.58MHz         wait valid sync (150 ms)
B0012      00B6      BOTIME EQU    >B6    3.58MHz         BOT past head (300 ms)
 0235                *      COPY   ALC.JCF.STRINGY.SRC.MHZ5
 0236                *-------------------------------------------------------
 0237                *      COPY   ALC.JCF.STRINGY.SRC.FE
 0238                       COPY   ALC.JCF.STRINGY.SRC.PE
C0001                * interrupt select & clear constant equates
C0002      0043      I1CS   EQU    >43                    clear and select INT1
C0003      006A      I123C  EQU    >6A                    clear INT1,2&3 flags
C0004      0048      I2C    EQU    >48                    clear INT2 flag
C0005      004C      I2CS   EQU    >4C                    clear and select INT2
C0006      0004      I2S    EQU    >04                    test INT2 select bit
C0007      0068      I23C   EQU    >68                    clear INT2&3 flags
C0008      007C      I23CS  EQU    >7C                    clear and select INT2&3
C0009      0060      I3C    EQU    >60                    clear INT3 flag
C0010      0070      I3CS   EQU    >70                    clear and select INT3
```